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# SiGe(C) epitaxial technologies—issues and perspectives

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## Abstract

Epitaxial layers of SiGe(C) have entered mainstream Si processing—forming base regions in heterojunction bipolar transistors. There are also exciting prospects that SiGe(C) could impact MOS technologies. In both cases heteroepitaxial layers enable very significant performance enhancements at device and circuit level. A related area and a familiar hot-potato is silicon epitaxy for device active regions in MOS technologies—where tightly controlled doping distributions can be incorporated to facilitate device function at deep submicron channel lengths. CVD is a preferred epitaxy deposition technique for production—currently LP-CVD and UHV-CVD dominate. Each of these techniques demand much of the technology and have their respective strengths and weaknesses. Issues regarding matrix and doping control, uniformity, blanket and selective area growth and throughput (a sensitive area) will be addressed. Also in the CVD portfolio is LEPE-CVD—a recent contender for the production arena which has the facility of being able to access very high deposition rates as required for example in depositing relaxed buffer layer material required as ‘virtual substrates’ for higher Ge content layers. SS-MBE, traditionally the favourite technique for research, also has distinct possibilities for development as a production tool. Here the issues relate primarily to throughput and system design, and (surprisingly) matrix profile control. These techniques will be outlined and reviewed along with issues which determine their development as the competition heats up in epitaxy, and as more complex and high Ge content structures are needed to progress Si technology to new performance heights and application areas. © 2002 Elsevier Science B.V. All rights reserved.

**Keywords:** SiGe epitaxy; Layer growth techniques; Device technologies

## 1. Introduction

Epitaxy is playing an increasingly significant role in Si microelectronics. CMOS integrated circuits (ICs) are fabricated in Si ‘epi’ and advanced bipolar junction transistors (BJTs) have epitaxial base regions. An important recent development has been the entry of the SiGe heterojunction bipolar transistors (HBT) into the production arena—devices which significantly outperform Si BJTs, and which demand much of the epitaxy process, with  $z$  control of matrix and dopant concentrations down to nanometre dimensions. The addition of C to the base region to suppress B diffusion adds a further dimension on epitaxy growth and control.

The SiGe devices are fabricated using near conventional Si processing techniques, and crucially, in the case of SiGe BiCMOS, have to be processed alongside Si CMOS circuitry, again putting demands on the epi process. There is also an intriguing possibility that SiGe can similarly be used to enhance MOSFET device performance, and epitaxy may also find a role in

defining high resolution dopant structures required in advanced sub 100 nm CMOS technologies.

In this paper we review the approaches being made in production environments to fabricate SiGe(C) epitaxial device structures and consider what further developments are possible in this exciting and challenging area.

## 2. Chemical vapour deposition

Chemical vapour deposition (CVD) is currently being used, almost exclusively, by process engineers as the growth technology for SiGe(C) heterojunction device material. CVD has been used for over two decades for Si epitaxial growth—generally a few micrometres of material for CMOS ICs. CVD techniques have been developed over this time to yield today’s sophisticated single-wafer tool, currently operating with 8 inch wafers but a 12-inch capability exists.

CVD depends on thermally-induced chemical interactions at the Si wafer surface as a means of depositing epitaxial material (see Fig. 1). Suitable mixtures of so-called precursors (source gases) containing atoms of interest are carried (usually with  $H_2$  carrier gas) over the Si wafer [1]. Crucial operating parameters include

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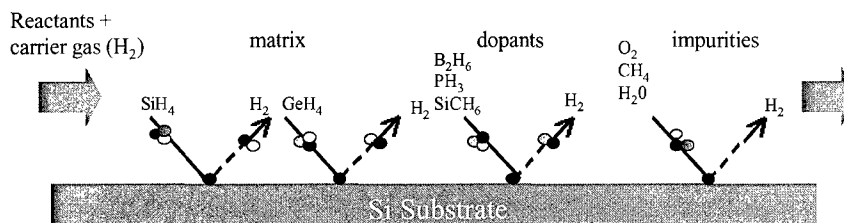


Fig. 1. Schematic representation of the thermally activated chemical decomposition of incident precursors, leading to growth of SiGe:C by the LP-CVD process. Impurities shown are unintentional but can influence growth at low temperatures.

wafer temperature, pressure and flow rate and purity of the gaseous mixture. The challenges presented by Si heterostructures require additionally the ability to incorporate very abrupt compositional changes in this process and over the last decade this has led to the cold-walled low pressure (LP)-CVD variant being developed where pressures are reduced typically from 100s to 10s of torr pressure, and growth temperatures from typically 950–650 °C.

### 2.1. SiGe(C) LP-CVD

Si/Si<sub>1-x</sub>Ge<sub>x</sub> is essentially a strained layer technology and this requires lower growth temperatures than used in Si homoepitaxy to preserve strain and to suppress development of elastic relaxation processes, enabling highly planar structures to be grown. Temperatures of approximately 650 °C are used for the growth of  $x=0.2$  structures. In this regime the growth rate becomes temperature limited (see Fig. 2), allowing source gas (typically SiH<sub>4</sub> and GeH<sub>4</sub>) pressures to be reduced and

to thereby minimise disruption in the growth arising from turbulence. However, because sharp interfaces are generally required high flow rates (carrier gas + source gases) are used to enable rapid changes in the composition of the gas over the wafer to be achieved.

Operating in this regime, however, has a downside. Growth rates are low with implications on throughput and because we are acting with an activated decomposition process, growth rate depends critically on temperature (see Fig. 2). At 650 °C a change of 1 °C will alter the deposition rate by ~10%—well outside the specification demanded by process engineers! The wafer temperature therefore has to be highly reproducible and highly uniform across the wafer-demanding complex heater technology designed just to heat the wafer and its holder (susceptor), sophisticated temperature measurement system and operational procedures. Temperature measurements down to these low temperatures have proved to be difficult, and currently wafer temperature is monitored (rather than directly measured) by either pyrometers or thermocouples mounted in the susceptor

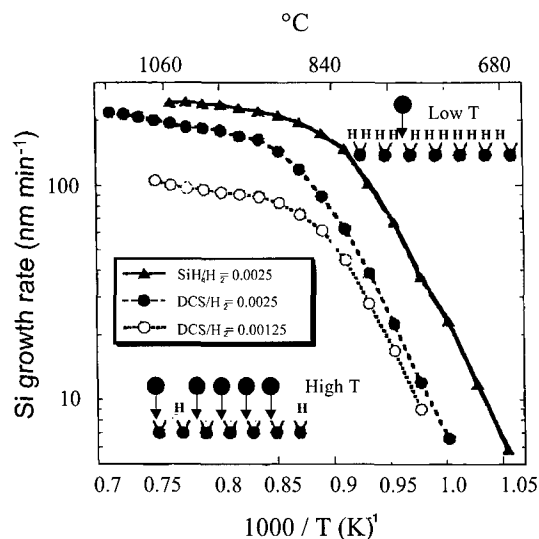


Fig. 2. Temperature dependence on the Si growth rate for different precursors/gas flow rates during the LP-CVD process, indicating an activated decomposition process for growth temperatures ( $T_G$ ) < 800 °C. The insets show flow rate limited growth at high  $T_G$  and temperature limited growth at low  $T_G$ .

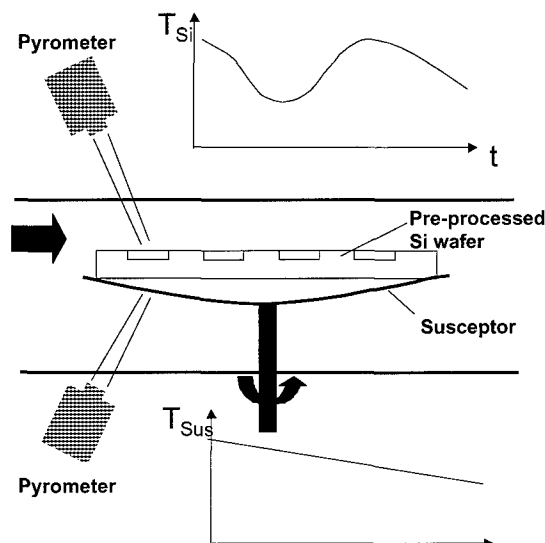


Fig. 3. Schematic representation of the sample susceptor, showing differences in susceptor to wafer temperature with time, due to coating of the susceptor and emissivity changes and possible temperature variations in the reactor.

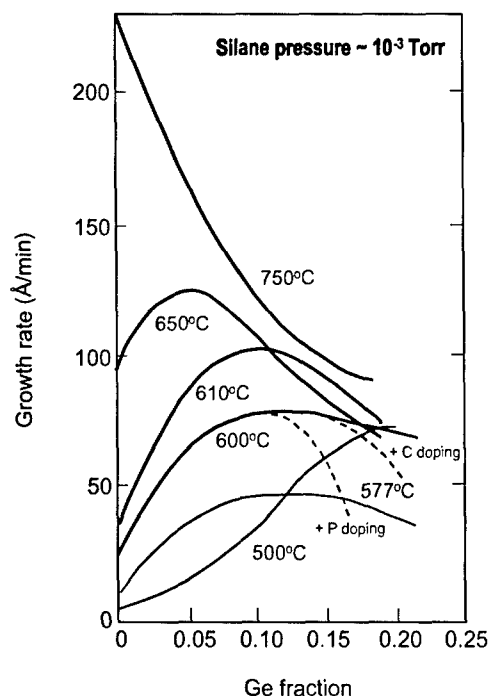


Fig. 4. Interdependence of growth rate and Ge fraction—further complicated in the presence of dopants for various deposition temperatures.

which holds the wafer (see Fig. 3). As all heating is accomplished by radiation, changes in the emissivity of the wafer holder and surrounding infrastructure which can occur during deposition, means that this is at best only an indicator of wafer temperature. This situation is further complicated by actual temperature changes on the surface of the grown layer-induced by emissivity changes produced by compositional changes in the growing layer or changes in surface topography or arising from any pre-processing carried out on the wafer.

It is thus evident that a considerable amount of process development is required in LP-CVD reactors—very iterative in nature—to yield a prescribed heterostructure design. These procedures are further complicated by the interdependence of the deposition rates at the surface—for example, deposition rates of 650 °C are reduced by Ge for  $x$  up to 0.05 and then decrease quite dramatically with increasing value of  $x$  (see Fig. 4). It is a tribute therefore that Osten and co-workers at IHP have developed a process involving source gas methyl/silane, to yield C concentrations of  $10^{19}$ – $10^{20}$  cm<sup>-3</sup> in a B-doped SiGe base of the HBT, to suppress B diffusion [2].

Also as growth temperatures are reduced it becomes increasingly difficult to maintain clean deposition conditions. Water and oxygen (especially) in the background ambient produce oxidation followed by desorption as volatile SiO. As temperatures are reduced significant reductions in background contamination pres-

ures are required to maintain an oxide-free surface, so procedures have to be developed which minimise such oxidation (Fig. 5). This is especially difficult at the wafer cleaning stage, which involves a high temperature bake (between 700 and 900 °C) usually in the presence of hydrogen to generate a clean surface, and exposure to the background ambient before growth can be commenced leads to some oxidation of the surface.

Process development is the 'Achilles heel' of the LP-CVD process, especially as there is always pressure to keep throughput (wafers per hour) at acceptable levels. Wafer cleaning procedures are being developed to increase throughput and maintain wafer cleanliness prior to epi deposition. With wafer temperature excursions (e.g. cleaning → deposition) time has to be allowed for wafer temperatures to settle with obvious penalties on throughput. Good practise in LP-CVD also entails cleaning the reactor before the next wafer is introduced—involving pushing HCl through the system, again with throughput implications. This leaves the system cleansed of previously deposited material to facilitate reproducible temperature measurement and eliminate memory doping problems. However, once the entire process has been developed, LP-CVD reactors offer the industry very reliable and reproducible 'blanket' (i.e. covering the entire wafer) SiGe(C) layer growth, with long campaign lengths, a material quality second to none and with layer thickness control demonstrated down to ~1 nm for  $x \approx 0.2$  (see Fig. 6).

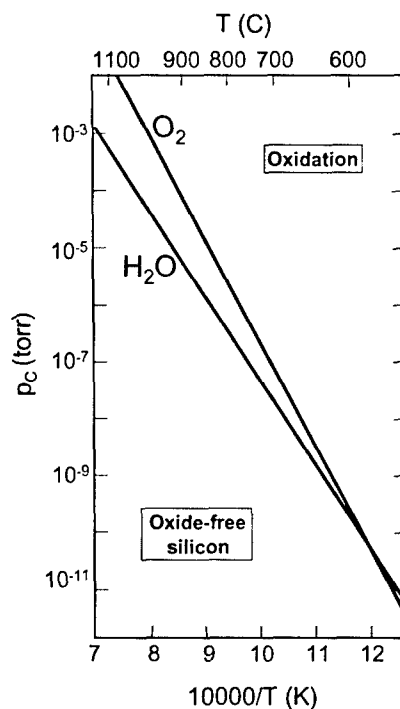


Fig. 5. Temperature dependence of H<sub>2</sub>O and O<sub>2</sub> pressures required to maintain an oxide free surface.

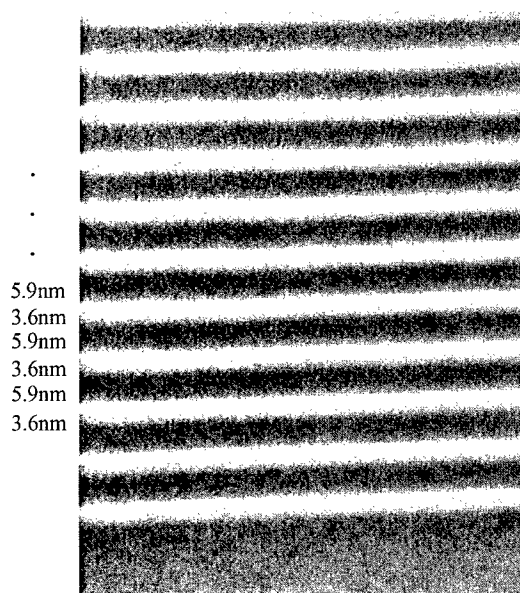


Fig. 6. Bright field cross-sectional (XTEM) micrograph of multiple quantum well (QW) structure for Ge fraction ( $x$ )=0.2 grown by LP-CVD (showing 'state of the art' highly planar (1 nm resolution) interfaces).

Selective epi growth (SEG) in silicon 'windows' defined usually by  $\text{SiO}_2$  patterns is a very challenging adaptation of the LP-CVD process—but can have significant processing advantages. This is achieved by adding gaseous HCl to the gas mixture, but selectively imposes further limitation of the process 'window'. SEG is a hot research topic in several large institutions.

## 2.2. UHV-CVD

In the late 1980s Berni Meyerson of IBM developed a radical new approach to the growth of Si/SiGe heterostructures. The underlining philosophy was that since very close control of heterointerfaces is required to yield high resolution compositional profiles, slow growth rates are indeed desirable, so that low temperature deposition must be confronted [3]. Meyerson chose 550 °C as the temperature, giving Si growth rates of  $\sim 0.3$  nm/min, with wafers immersed in a hot-walled (wafer temperature–wall temperature) furnace, giving highly uniform temperature across the wafer (Fig. 7). The growth pressure is also an important parameter to be considered, bearing in mind that in order to meet acceptable throughput levels, batch processing was essential with a large number of wafers (up to 35) required to meet throughput demands. The growth (total) pressure was reduced to very low levels— $10^{-3}$  torr to reduce unwanted silane chemistry reactions and crucially, to ensure a uniform material supply to the closely spaced wafers through molecular transport processes that occur at these pressures. Two other develop-

ments are necessary to reduce background gas pressures to UHV levels so that clean surface and deposition conditions could be ensured. An ex-situ wafer cleaning process was also developed involving H termination of surface bonds to dramatically reduce oxidation, and enable the generation of clean surfaces at 550 °C.

UHV-CVD technology is used primarily by IBM and yields exceedingly high quality and highly uniform heterostructure layers with throughput acceptable to a BiCMOS production line at IBM.

## 2.3. LEPE-CVD

With HBT devices the strained heterolayers are grown directly on the Si wafer. However, full exploitation of the Si/SiGe technology requires substrate templates with lattice constants between Si and Ge to set the strain condition and also allow higher Ge content structures to be grown. Such substrates are termed 'virtual substrates' (VSs) and are fabricated by growing fully relaxed SiGe layers on the Si wafer. There have been several approaches to produce optimum VSs and the most studied is to gradually grade the Ge composition from 0 up to the desired value ( $y$ ) over several microns of material—this produces a well relaxed VS. However, a cross-hatch topographical structure usually develops on the surface as a consequence of dislocations interacting and is detrimental to the overgrowth of high quality active structures. Recently CMP processes have been developed which smooth out the VS.

A very recent development in CVD especially relevant to VS production, is low energy plasma-enhanced (LEPE-CVD) [4]. With this version of the CVD process, deposition takes place on a wafer immersed in an argon plasma and where with the biasing is such that argon ions impinging the substrate do no significant damage. The ions, however, modify the surface reaction chemistry to yield dramatically increased deposition rates—

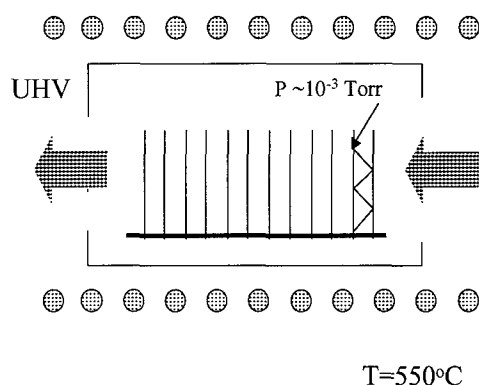


Fig. 7. Schematic of the 'hot wall' UHV-CVD reactor. The low pressure of gases ensures uniform material supply over the wafers by molecular flow.

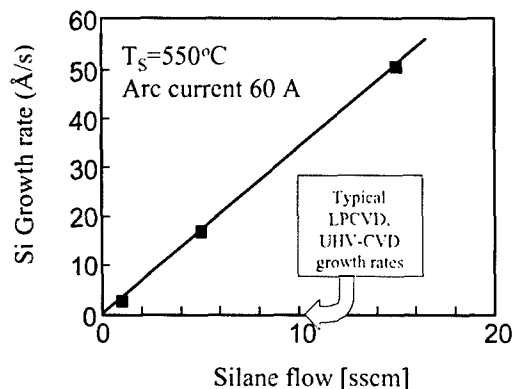


Fig. 8. Si growth rate dependence on the Silane flow for LEPE-CVD using a plasma arc current of 60 A at a growth temperature of 550 °C—indicating dramatic enhancement compared to conventional CVD.

approximately 100 times faster than conventional CVD at 550 °C (see Fig. 8).

LEPE-CVD has been able to produce high quality VS structures with very smooth surfaces in ~10 min as opposed to ~hours needed in LP-CVD, with corresponding economic implications. This opens up the possibility of using VS as the starting wafer (possibly with CMP) and with growth of the active heterostructures by another technique (e.g. LP-CVD). A further intriguing development by von Kanel at ETH (Zurich) has been to reduce (by deflection) the plasma density at the substrate and thereby back-off the deposition rate in LEPE-CVD to approximately 0.1 nm/s, allowing active layer (~8 nm thick) deposition on the freshly grown VS. Already, very high quality Si p-channel MOSFET device structures have been fabricated in material grown using such an approach (Fig. 9).

#### 2.4. Role of SS-MBE

The question arises, particularly pertinent to this conference, does solid source (SS)-MBE have any significant role to play in Si/SiGe heterostructure production? MBE is viewed by the Si industry as a good research tool, but with its UHV operating conditions, and the limited source supply (re e-beam evaporation sources), the industry considers that it is not process-friendly or able to reach throughputs levels needed in production.

As the growth temperatures in CVD are reduced, however, to accommodate strain layer growth, deposition rates quickly fall off and the 6–30 nm/min available in SS-MBE start to look respectable. In addition, because MBE is a physical deposition process the deposition rate of all components and deposition temperature are decoupled. This is certainly a considerable attribute when developing processes, and unlike CVD, MBE is easily capable of delta layer deposition and also of high

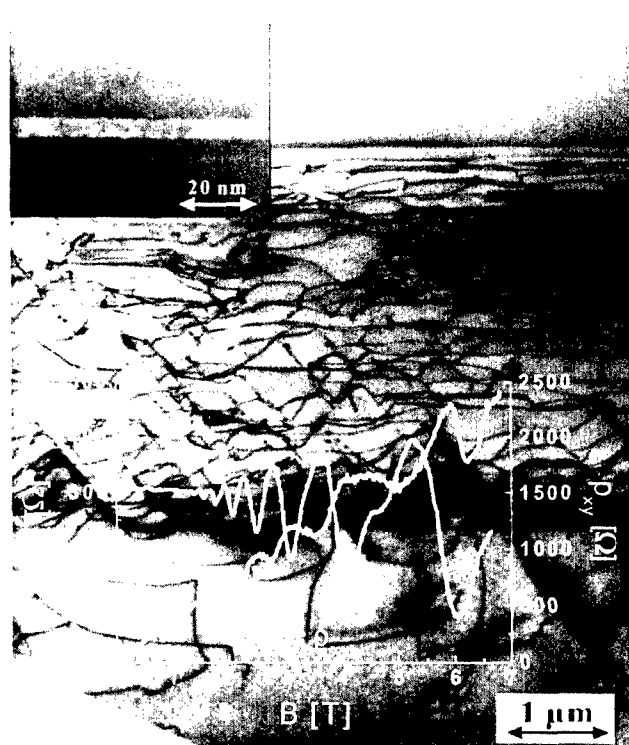


Fig. 9. Cross-sectional (XTEM) dark field micrograph of a p-channel MOSFET structure grown by LEPE-CVD. The virtual substrate (VS) was grown at a high deposition rate (~15 min)—plasma density reduced for channel region to obtain high interfacial definition.

Ge content ( $0.4 < x < 1$ ) layers (e.g. see Fig. 10) which may well be needed in future HBT devices and SiGe MOSFETs. Mechanical flux shutters allow for exceedingly precise control of deposited material. The demands placed on substrate temperature are much less stringent

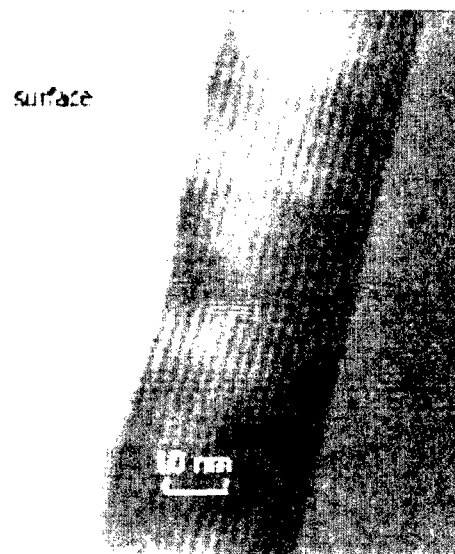


Fig. 10. Cross-sectional (XTEM) bright field micrograph of a SiGe superlattice grown by SS-MBE showing alternate 1 nm Si–Ge layers.

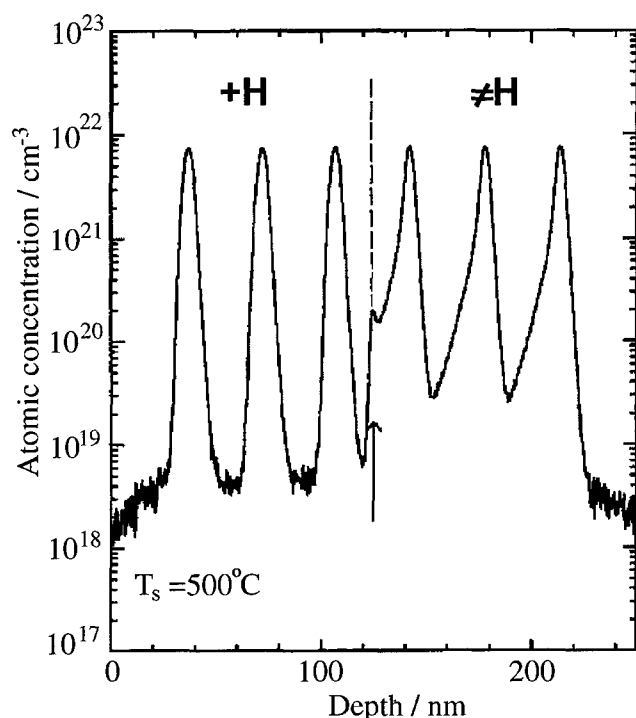


Fig. 11. Ge secondary ion mass spectroscopy (SIMS) profiles showing how  $H^+$  surfactants can be used to suppress Ge segregation in SS-MBE.

than in CVD, leading to a much simpler heater system and temperature stabilisation regimes. However, there are some growth temperatures where segregation of matrix and dopant species (Ge, B, Sb) can be more prevalent than in CVD and this could be restrictive, although procedures are being developed which reduced segregation to CVD levels [5] (Fig. 11). A further issue is that with the current technology only approximately 15% of the evaporated Si and Ge fluxes are used for layer growth on the wafer, the remainder deposited over the system infrastructure. This excess material then

would require proper management if it is not to lead to particle contamination of the system and the wafer [6].

### 3. Conclusions

In this review we have attempted to address the critical issues for epitaxy technologies as epitaxy becomes an exceedingly significant process in Si micro-electronics. Without doubt variants of the CVD process seem to have a secure future. Once the process has been developed it really comes into its own—with long-term campaign times, high reproducibility and high material quality. In LP-CVD, the principal tool in the field, the critical dependence of deposition rates on growth temperature, means that careful management of the system is required to maintain reliability of layer specifications. UHV-CVD, with its hot-wall reaction chamber allows wafers to be immersed in a thermal enclosure giving excellent uniformity and quality. However, great demands are placed on both these techniques as new structures are needed to continually improve device performance. It is possible that new precursors will become available to improve deposition rates at low temperature. LEPE-CVD, a relative newcomer to the field, may well prove to be of great significance for low temperature deposition and a full appraisal of these techniques is eagerly awaited. Some radical developments in SS-MBE technology will be needed before that could be considered to enter the production arena.

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